

Control Integrated POver System (CIPOS™)

IGCM06G60GA

Datasheet

Table of Contents

| | |
|--------------------------------------------------------------------------------------|-----------|
| CIPOS™ Control Integrated POver System | 3 |
| Features | 3 |
| Target Applications..... | 3 |
| Description | 3 |
| System Configuration..... | 3 |
| Pin Configuration | 4 |
| Internal Electrical Schematic | 4 |
| Pin Assignment | 5 |
| Pin Description | 5 |
| HIN(U, V, W) and LIN(U, V, W) (Low side and high side control pins, Pin 7 - 12)..... | 5 |
| VFO (Fault-output and NTC, Pin 14) | 6 |
| ITRIP (Over current detection function, Pin 15)..... | 6 |
| VDD, VSS (Low side control supply and reference, Pin 13, 16)..... | 6 |
| VB(U, V, W) and VS(U, V, W) (High side supplies, Pin 1 - 6)..... | 6 |
| N (Low side common emitter, Pin 17 - 19) | 6 |
| W, V, U (High side emitter and low side collector, Pin 20 - 22) | 6 |
| P (Positive bus input voltage, Pin 23)..... | 6 |
| Absolute Maximum Ratings | 7 |
| Module Section | 7 |
| Inverter Section..... | 7 |
| Control Section | 7 |
| Recommended Operation Conditions | 8 |
| Static Parameters | 9 |
| Dynamic Parameters | 10 |
| Bootstrap Parameters | 10 |
| Thermistor | 11 |
| Mechanical Characteristics and Ratings | 11 |
| Circuit of a Typical Application | 12 |
| Switching Times Definition | 13 |
| Electrical characteristic | 14 |
| Package Outline | 15 |
| Revision History | 16 |

CIPOS™

Control Integrated POver System

Dual In-Line Intelligent Power Module
3Φ-bridge 600V / 6A

Features

Fully isolated Dual In-Line molded module

- Reverse conducting IGBTs with monolithic body diode
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11V for signal transmission at VBS=15V
- Integrated bootstrap functionality
- Over current shutdown
- Temperature monitor
- Under-voltage lockout at all channels
- Low side common emitter
- Cross-conduction prevention
- All of 6 switches turn off during protection
- Lead-free terminal plating; RoHS compliant

Target Applications

- Dish washers
- Refrigerators
- Fans
- Low power motor drives

Description

The CIPOS™ module family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

It is designed to control three phase AC motors and permanent magnet motors in variable speed drives for applications like a refrigerator and a dish washer. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also EMI-save control and overload protection.

The reverse conducting IGBTs are combined with an optimized SOI gate driver for excellent electrical performance.

System Configuration

- 3 half bridges with reverse conducting IGBTs
- 3Φ SOI gate driver
- Thermistor
- Pin-to-heatsink clearance distance typ. 1.6mm

Pin Configuration

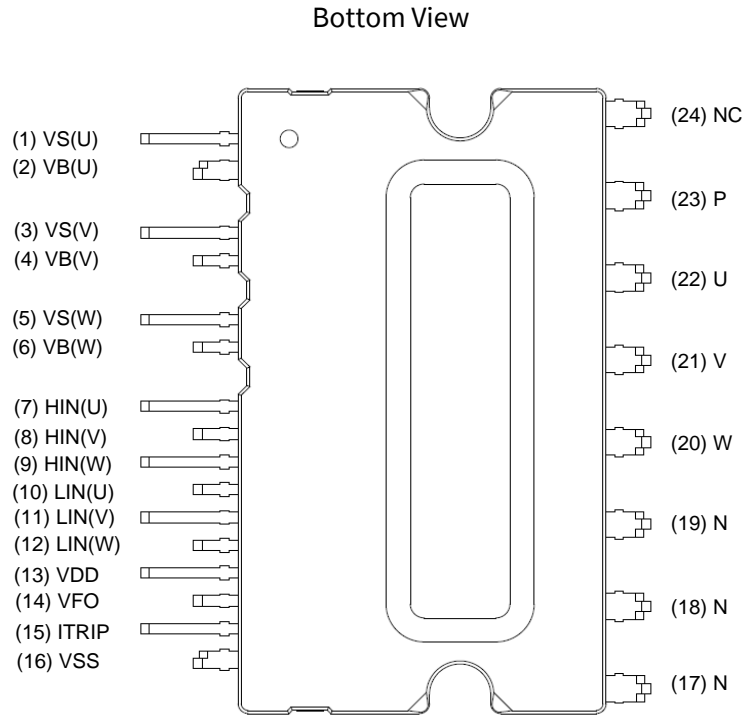


Figure 1 Pin configuration

Internal Electrical Schematic

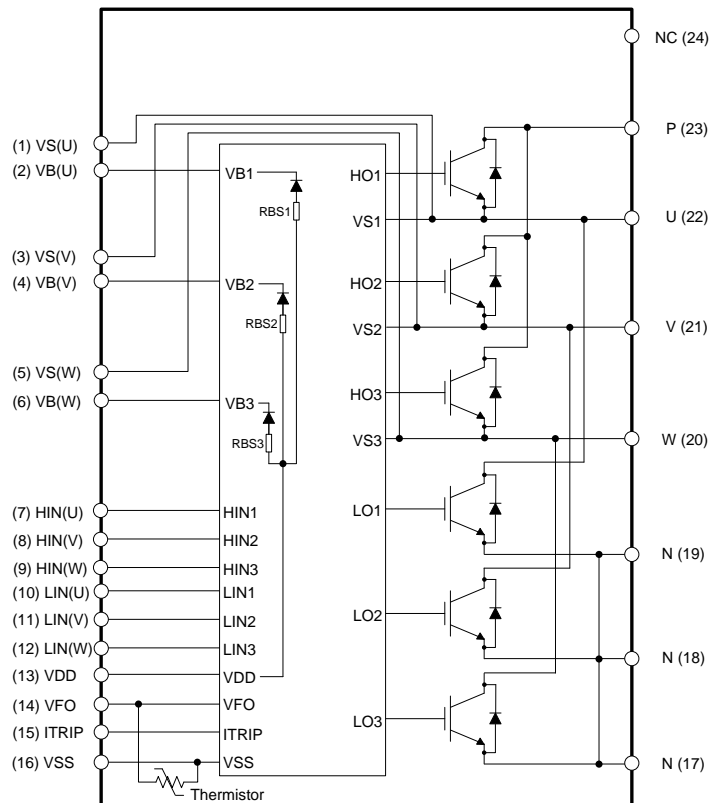


Figure 2 Internal schematic

Pin Assignment

| Pin Number | Pin Name | Pin Description |
|------------|----------|-----------------------------------------------------|
| 1 | VS(U) | U-phase high side floating IC supply offset voltage |
| 2 | VB(U) | U-phase high side floating IC supply voltage |
| 3 | VS(V) | V-phase high side floating IC supply offset voltage |
| 4 | VB(V) | V-phase high side floating IC supply voltage |
| 5 | VS(W) | W-phase high side floating IC supply offset voltage |
| 6 | VB(W) | W-phase high side floating IC supply voltage |
| 7 | HIN(U) | U-phase high side gate driver input |
| 8 | HIN(V) | V-phase high side gate driver input |
| 9 | HIN(W) | W-phase high side gate driver input |
| 10 | LIN(U) | U-phase low side gate driver input |
| 11 | LIN(V) | V-phase low side gate driver input |
| 12 | LIN(W) | W-phase low side gate driver input |
| 13 | VDD | Low side control supply |
| 14 | VFO | Fault output / Temperature monitor |
| 15 | ITRIP | Over current shutdown input |
| 16 | VSS | Low side control negative supply |
| 17, 18, 19 | N | Low side common emitter |
| 20 | W | Motor W-phase output |
| 21 | V | Motor V-phase output |
| 22 | U | Motor U-phase output |
| 23 | P | Positive bus input voltage |
| 24 | NC | No Connection |

Pin Description

HIN(U, V, W) and LIN(U, V, W) (Low side and high side control pins, Pin 7 - 12)

These pins are positive logic and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-down resistor of about 5kΩ is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time t_{FILIN} . The filter acts according to Figure 4.

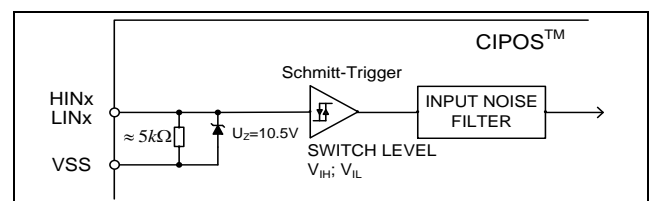


Figure 3 Input pin structure

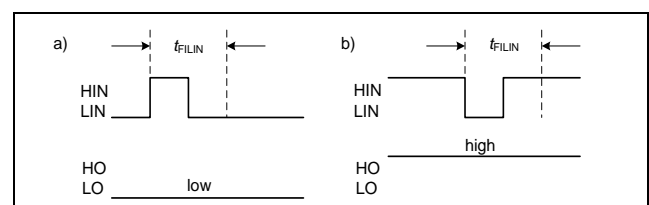


Figure 4 Input filter timing diagram

It is not recommended for proper work to provide input pulse-width lower than 1µs.

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 380ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

VFO (Fault-output and NTC, Pin 14)

The VFO pin indicates a module failure in case of under voltage at pin VDD or in case of triggered over current detection at ITRIP. A pull-up resistor is externally required.



Figure 5 Internal circuit at pin VFO

The same pin provides direct access to the NTC, which is referenced to VSS. An external pull-up resistor connected to +5V ensures that the resulting voltage can be directly connected to the microcontroller.

ITRIP (Over current detection function, Pin 15)

CIPOS™ provides an over current detection function by connecting the ITRIP input with the IGBT collector current feedback. The ITRIP comparator threshold (typ. 0.47V) is referenced to VSS ground. An input noise filter (typ.: $t_{ITRIPMIN} = 530ns$) prevents the driver to detect false over-current events.

Over current detection generates a shutdown of all outputs of the gate driver after the shutdown propagation delay of typically 1000ns.

The fault-clear time is set to minimum 40µs.

VDD, VSS (Low side control supply and reference, Pin 13, 16)

VDD is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to VSS ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+} = 12.1V$ is present.

The IC shuts down all the gate drivers power outputs, when the VDD supply voltage is below $V_{DDUV-} = 10.4V$. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB(U, V, W) and VS(U, V, W) (High side supplies, Pin 1 - 6)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+} = 12.1V$ and a falling threshold of $V_{BSUV-} = 10.4V$.

VS(U, V, W) provide a high robustness against negative voltage in respect of VSS of -50V transiently. This ensures very stable designs even under rough conditions.

N (Low side common emitter, Pin 17 - 19)

The low side common emitter is available for current measurement. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

W, V, U (High side emitter and low side collector, Pin 20 - 22)

These pins are motor U, V, W input pins.

P (Positive bus input voltage, Pin 23)

The high side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450V.

Absolute Maximum Ratings

($V_{DD} = 15V$ and $T_J = 25^\circ C$, if not stated otherwise)

Module Section

| Description | Condition | Symbol | Value | | Unit |
|----------------------------------|------------------------------|------------|-------|-----|------------|
| | | | min | max | |
| Storage temperature range | | T_{stg} | -40 | 125 | $^\circ C$ |
| Isolation test voltage | RMS, $f = 60Hz$, $t = 1min$ | V_{ISOL} | 2000 | - | V |
| Operating case temperature range | Refer to Figure 6 | T_C | -40 | 100 | $^\circ C$ |

Inverter Section

| Description | Condition | Symbol | Value | | Unit |
|-----------------------------------------------|---------------------------------------------------------------------------------|-----------------|----------|--------|------------|
| | | | min | max | |
| Max. blocking voltage | $I_C = 250\mu A$ | V_{CES} | 600 | - | V |
| DC link supply voltage of P-N | Applied between P-N | V_{PN} | - | 450 | V |
| DC link supply voltage (surge) of P-N | Applied between P-N | $V_{PN(surge)}$ | - | 500 | V |
| Output current | $T_C = 25^\circ C, T_J < 150^\circ C$ $T_C = 100^\circ C, T_J < 150^\circ C$ | I_C | -6 -4 | 6 4 | A |
| Maximum peak output current | less than 1ms | $I_{C(peak)}$ | -12 | 12 | A |
| Short circuit withstand time ¹ | $V_{DC} \leq 400V, T_J = 150^\circ C$ | t_{SC} | - | 5 | μs |
| Power dissipation per IGBT | | P_{tot} | - | 23.6 | W |
| Operating junction temperature range | | T_J | -40 | 150 | $^\circ C$ |
| Single IGBT thermal resistance, junction-case | | R_{thJC} | - | 5.3 | K/W |

Control Section

| Description | Condition | Symbol | Value | | Unit |
|-----------------------------------------------|-----------------|-------------------------|----------|----------|------|
| | | | min | max | |
| Module supply voltage | | V_{DD} | -1 | 20 | V |
| High side floating supply voltage (VB vs. VS) | | V_{BS} | -1 | 20 | V |
| Input voltage | LIN, HIN, ITRIP | V_{IN} V_{ITRIP} | -1 -1 | 10 10 | V |
| Switching frequency | | f_{PWM} | - | 20 | kHz |

¹ Allowed number of short circuits: <1000; time between short circuits: >1s.

Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

| Description | Symbol | Value | | | Unit |
|-------------------------------------------------------|-------------------|-------|-----|------|------------|
| | | min | typ | max | |
| DC link supply voltage of P-N | V_{PN} | 0 | - | 400 | V |
| High side floating supply voltage (V_B vs. V_S) | V_{BS} | 13.5 | - | 18.5 | V |
| Low side supply voltage | V_{DD} | 14.0 | 16 | 18.5 | V |
| Control supply variation | ΔV_{BS} , | -1 | - | 1 | V/ μ s |
| | ΔV_{DD} | -1 | - | 1 | |
| Logic input voltages LIN, HIN, ITRIP | V_{IN} | 0 | - | 5 | V |
| | V_{ITRIP} | 0 | - | 5 | |
| Between V_{SS} - N (including surge) | V_{SS} | -5 | - | 5 | V |

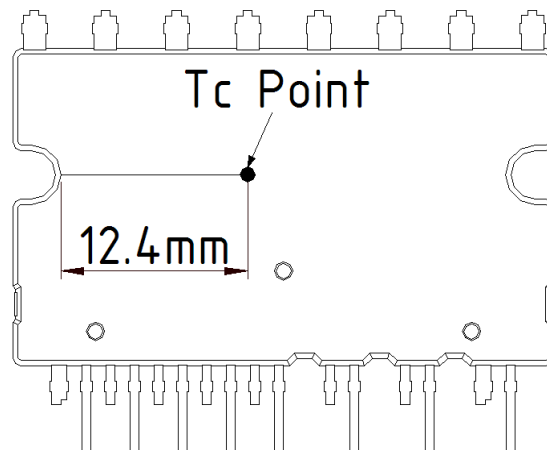


Figure 6 T_c measurement point¹

¹Any measurement except for the specified point in figure 6 is not relevant for the temperature verification and brings wrong or different information.

Static Parameters

($V_{DD} = 15V$ and $T_J = 25^\circ C$, if not stated otherwise)

| Description | Condition | Symbol | Value | | | Unit |
|-----------------------------------------------------------|---------------------------------------------------|----------------------------|--------|-------------|----------|---------|
| | | | min | typ | max | |
| Collector-Emitter saturation voltage | $I_C = 4A$ $T_J = 25^\circ C$ $150^\circ C$ | $V_{CE(sat)}$ | - - | 1.6 1.8 | 2.0 - | V |
| Emitter-Collector forward voltage | $I_F = 4A$ $T_J = 25^\circ C$ $150^\circ C$ | V_F | - - | 1.75 1.8 | 2.2 - | V |
| Collector-Emitter leakage current | $V_{CE} = 600V$ | I_{CES} | - | - | 1 | mA |
| Logic "1" input voltage (LIN, HIN) | | V_{IH} | - | 2.1 | 2.5 | V |
| Logic "0" input voltage (LIN, HIN) | | V_{IL} | 0.7 | 0.9 | - | V |
| ITRIP positive going threshold | | $V_{IT,TH+}$ | 400 | 470 | 540 | mV |
| ITRIP input hysteresis | | $V_{IT,HYS}$ | 40 | 70 | - | mV |
| VDD and VBS supply under voltage positive going threshold | | V_{DDUV+} V_{BSUV+} | 10.8 | 12.1 | 13.0 | V |
| VDD and VBS supply under voltage negative going threshold | | V_{DDUV-} V_{BSUV-} | 9.5 | 10.4 | 11.2 | V |
| VDD and VBS supply under voltage lockout hysteresis | | V_{DDUVH} V_{BSUVH} | 1.0 | 1.7 | - | V |
| Input clamp voltage (HIN, LIN, ITRIP) | $I_{in} = 4mA$ | $V_{INCLAMP}$ | 9.0 | 10.1 | 12.5 | V |
| Quiescent V_{Bx} supply current (V_{Bx} only) | $H_{IN} = 0V$ | I_{QBS} | - | 300 | 500 | μA |
| Quiescent VDD supply current (VDD only) | $L_{IN} = 0V, H_{INX} = 5V$ | I_{QDD} | - | 370 | 900 | μA |
| Input bias current | $V_{IN} = 5V$ | I_{IN+} | - | 1 | 1.5 | mA |
| Input bias current | $V_{IN} = 0V$ | I_{IN-} | - | 2 | - | μA |
| ITRIP input bias current | $V_{ITRIP} = 5V$ | I_{ITRIP+} | - | 65 | 150 | μA |
| VFO input bias current | $VFO = 5V, V_{ITRIP} = 0V$ | I_{FO} | - | 60 | - | μA |
| VFO output voltage | $I_{FO} = 10mA, V_{ITRIP} = 1V$ | V_{FO} | - | 0.5 | - | V |

Dynamic Parameters

($V_{DD} = 15V$ and $T_J = 25^\circ C$, if not stated otherwise)

| Description | Condition | Symbol | Value | | | Unit |
|----------------------------------------------------------|------------------------------------------------------------------|----------------|-------|------|-----|---------|
| | | | min | typ | max | |
| Turn-on propagation delay time | $V_{LIN, HIN} = 5V,$ $I_C = 4A,$ $V_{DC} = 300V$ | t_{on} | - | 650 | - | ns |
| Turn-on rise time | | t_r | - | 20 | - | ns |
| Turn-on switching time | | $t_{c(on)}$ | - | 100 | - | ns |
| Reverse recovery time | | t_{rr} | - | 130 | - | ns |
| Turn-off propagation delay time | $V_{LIN, HIN} = 0V,$ $I_C = 4A,$ $V_{DC} = 300V$ | t_{off} | - | 680 | - | ns |
| Turn-off fall time | | t_f | - | 180 | - | ns |
| Turn-off switching time | | $t_{c(off)}$ | - | 220 | - | ns |
| Short circuit propagation delay time | From $V_{IT, TH+}$ to 10% I_{SC} | t_{SCP} | - | 1420 | - | ns |
| Input filter time ITRIP | $V_{ITRIP} = 1V$ | $t_{ITRIPmin}$ | - | 530 | - | ns |
| Input filter time at LIN, HIN for turn on and off | $V_{LIN, HIN} = 0V \& 5V$ | t_{FILIN} | - | 290 | - | ns |
| Fault clear time after ITRIP-fault | $V_{ITRIP} = 1V$ | t_{FLTCLR} | 40 | 65 | 200 | μs |
| Deadtime between low side and high side | | DT_{PWM} | 1.0 | - | - | μs |
| Deadtime of gate drive circuit | | DT_{IC} | - | 380 | - | ns |
| IGBT turn-on energy (includes reverse recovery of diode) | $V_{DC} = 300V, I_C = 4A$ $T_J = 25^\circ C$ $150^\circ C$ | E_{on} | - | 75 | - | μJ |
| | | | - | 130 | - | |
| IGBT turn-off energy | $V_{DC} = 300V, I_C = 4A$ $T_J = 25^\circ C$ $150^\circ C$ | E_{off} | - | 120 | - | μJ |
| | | | - | 190 | - | |
| Diode recovery energy | $V_{DC} = 300V, I_C = 4A$ $T_J = 25^\circ C$ $150^\circ C$ | E_{rec} | - | 40 | - | μJ |
| | | | - | 70 | - | |

Bootstrap Parameters

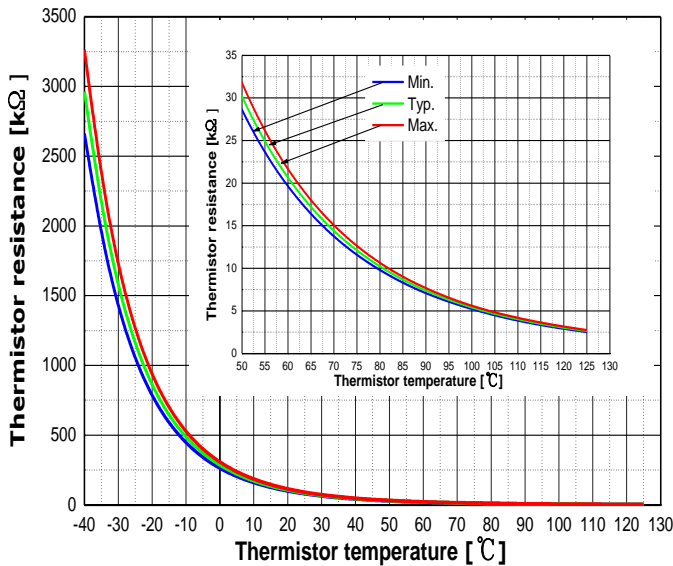
($T_J = 25^\circ C$, if not stated otherwise)

| Description | Condition | Symbol | Value | | | Unit |
|----------------------------------------------------|------------------------------------------|--------------|-------|-----|-----|----------|
| | | | min | typ | max | |
| Repetitive peak reverse voltage | | V_{RRM} | 600 | - | - | V |
| Bootstrap diode resistance of U-phase ¹ | $VS2$ or $VS3 = 300V, T_J = 25^\circ C$ | R_{BS1} | - | 35 | - | Ω |
| | $VS2$ and $VS3 = 0V, T_J = 25^\circ C$ | | | 40 | | |
| | $VS2$ or $VS3 = 300V, T_J = 125^\circ C$ | | | 50 | | |
| | $VS2$ and $VS3 = 0V, T_J = 125^\circ C$ | | | 65 | | |
| Reverse recovery time | $I_F = 0.6A, di/dt = 80A/\mu s$ | $t_{rr, BS}$ | - | 50 | - | ns |
| Forward voltage drop | $I_F = 20mA, VS2$ and $VS3 = 0V$ | $V_{F, BS}$ | - | 2.6 | - | V |

¹ R_{BS2} and R_{BS3} have same values to R_{BS1} .

Thermistor

| Description | Condition | Symbol | Value | | | Unit |
|---------------------------------------------------------|--------------------------------|-------------|-------|------|-----|------------------|
| | | | min | typ | max | |
| Resistor | $T_{NTC} = 25^{\circ}\text{C}$ | R_{NTC} | - | 85 | - | $\text{k}\Omega$ |
| B-constant of NTC (Negative Temperature Coefficient) | | $B(25/100)$ | - | 4092 | - | K |



| T [°C] | Rmin. [kΩ] | Rtyp. [kΩ] | Rmax. [kΩ] |
|--------|------------|------------|------------|
| 50 | 28.400 | 29.972 | 31.545 |
| 60 | 19.517 | 20.515 | 21.514 |
| 70 | 13.670 | 14.315 | 14.960 |
| 80 | 9.745 | 10.169 | 10.593 |
| 90 | 7.062 | 7.345 | 7.628 |
| 100 | 5.199 | 5.388 | 5.576 |
| 110 | 3.856 | 4.009 | 4.163 |
| 120 | 2.900 | 3.024 | 3.149 |
| 125 | 2.527 | 2.639 | 2.751 |

Figure 7 Thermistor resistance – temperature curve and table
(For more information, please refer to the application note ‘AN2016-10 CIPOS Mini Technical description’)

Mechanical Characteristics and Ratings

| Description | Condition | Value | | | Unit |
|-----------------|---------------------|-------|------|------|---------------|
| | | min | typ | max | |
| Mounting torque | M3 screw and washer | 0.59 | 0.69 | 0.78 | Nm |
| Flatness | Refer to Figure 8 | -50 | - | 100 | μm |
| Weight | | - | 6.15 | - | g |



Figure 8 Flatness measurement position

Circuit of a Typical Application

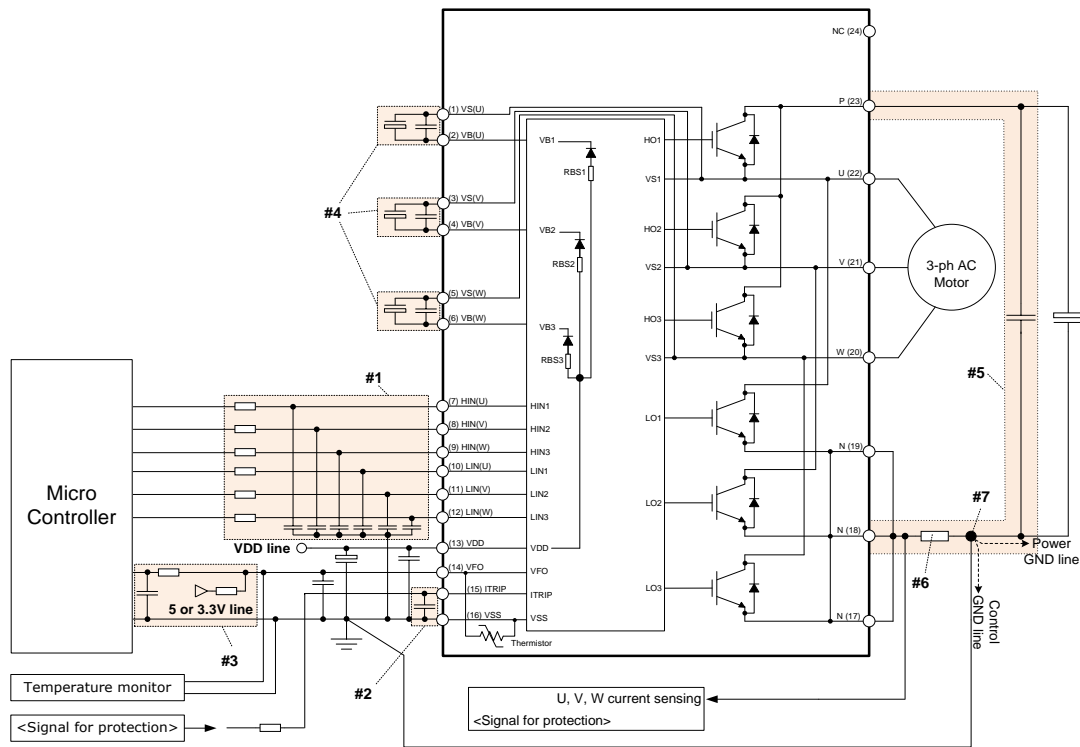


Figure 9 Typical application circuit

1. Input circuit

- To reduce input signal noise by high speed switching, the R_{IN} and C_{IN} filter circuit should be mounted. (100 Ω , 1nF)
- C_{IN} should be placed as close to V_{SS} pin as possible.

2. Itrip circuit

- To prevent protection function errors, C_{ITRIP} should be placed as close to Itrip and V_{SS} pins as possible.

3. VFO circuit

- VFO output is an open drain output. This signal line should be pulled up to the positive side of the 5V/3.3V logic power supply with a proper resistor R_{PU} .
- It is recommended that RC filter be placed as close to the controller as possible.

4. VB-VS circuit

- Capacitor for high side floating supply voltage should be placed as close to VB and VS pins as possible.

5. Snubber capacitor

- The wiring between CIPOS™ Mini and snubber capacitor including shunt resistor should be as short as possible.

6. Shunt resistor

- The shunt resistor of SMD type should be used for reducing its stray inductance.

7. Ground pattern

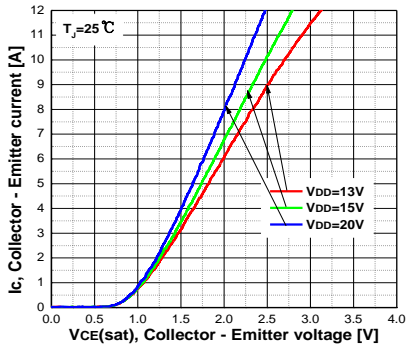
- Ground pattern should be separated at only one point of shunt resistor as short as possible.

Switching Times Definition

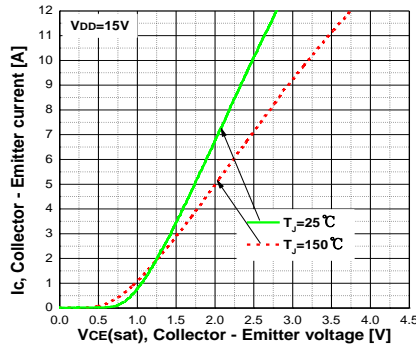


Figure 10 Switching times definition

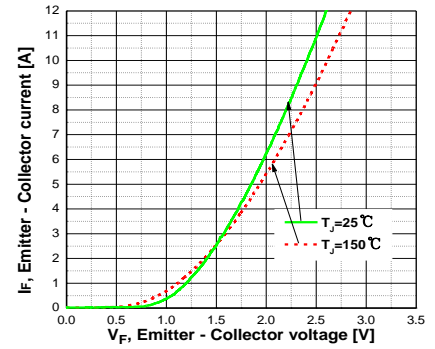
Electrical characteristic



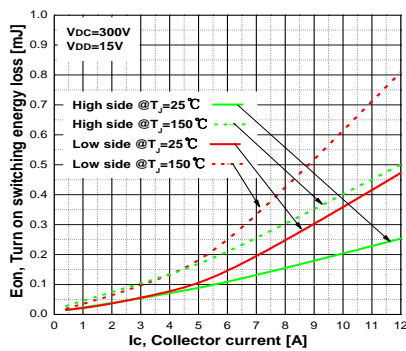
Typ. Collector – Emitter saturation voltage



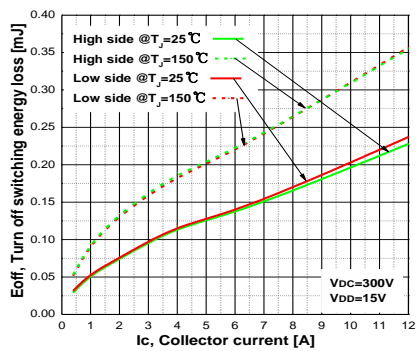
Typ. Collector – Emitter saturation voltage



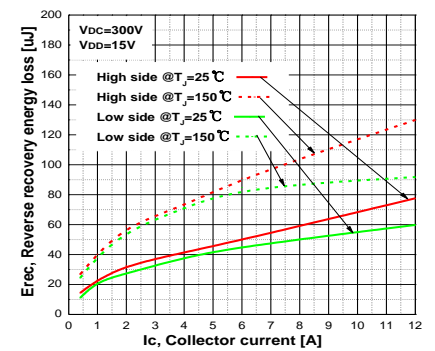
Typ. Emitter – Collector forward voltage



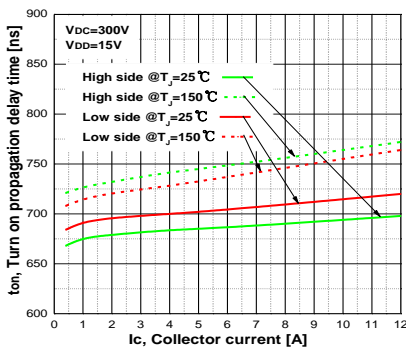
Typ. Turn on switching energy loss



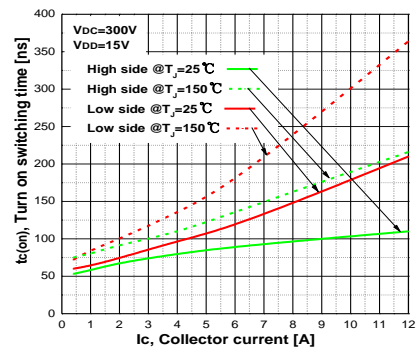
Typ. Turn off switching energy loss



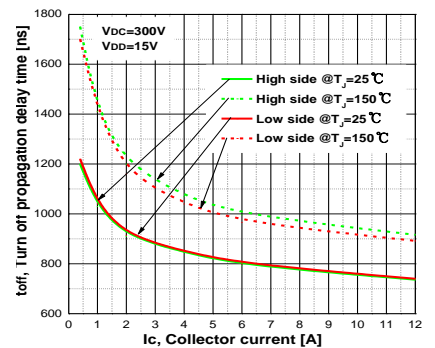
Typ. Reverse recovery energy loss



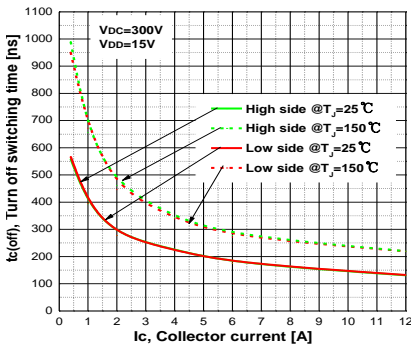
Typ. Turn on propagation delay time



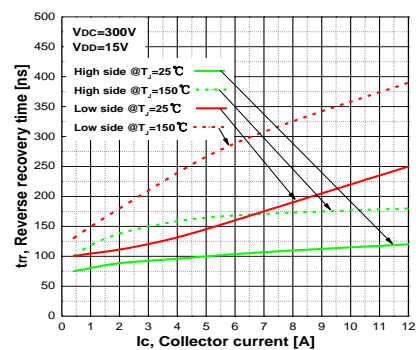
Typ. Turn on switching time



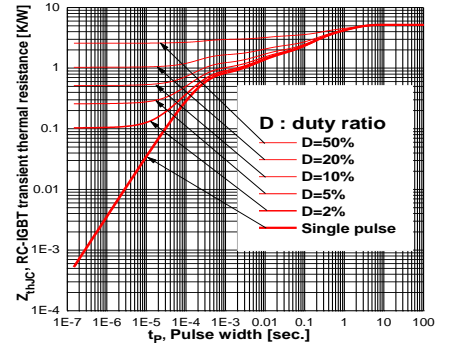
Typ. Turn off propagation delay time



Typ. Turn off switching time

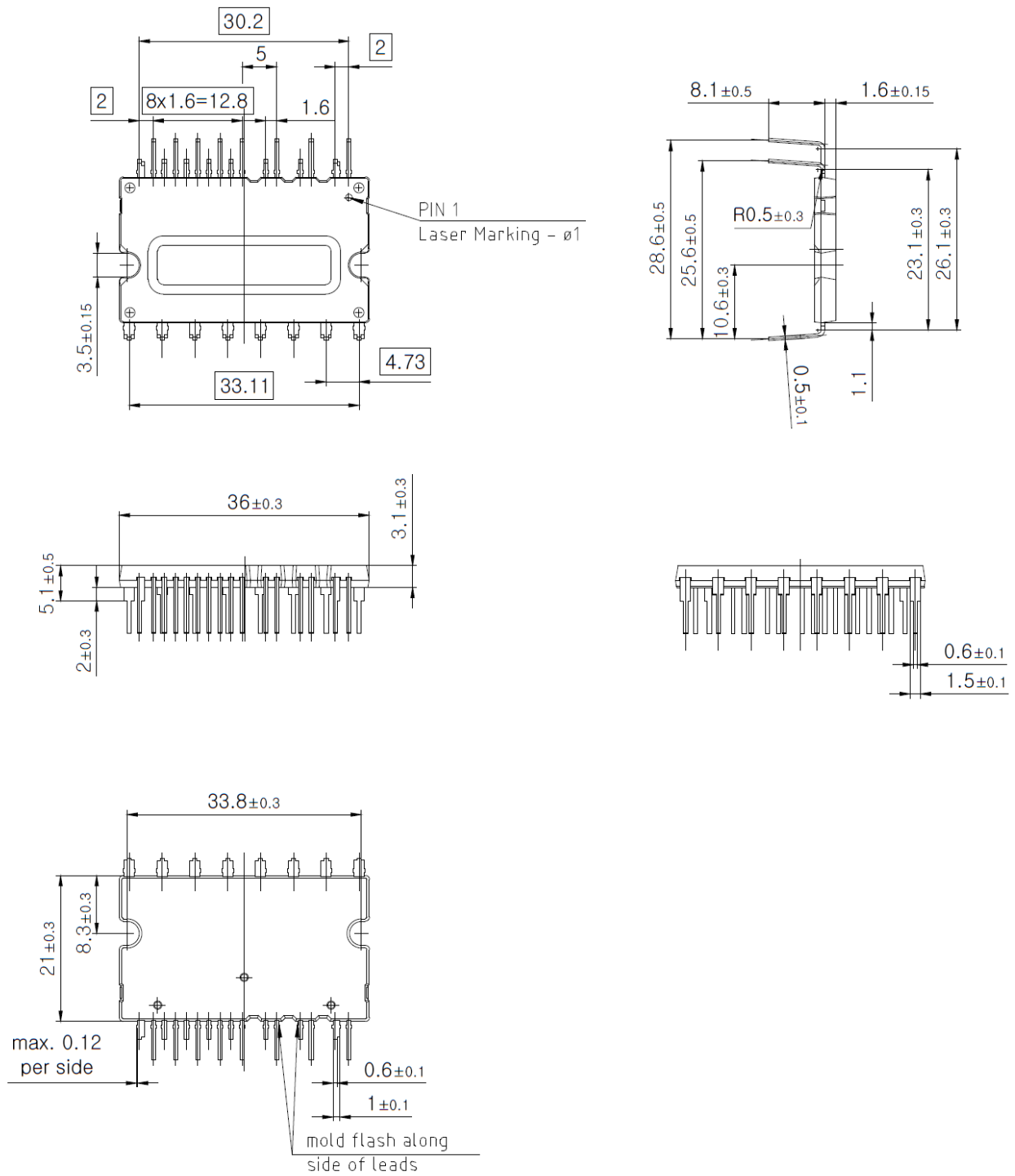


Typ. Reverse recovery time



IGBT transient thermal resistance at all six IGBTs operation

Package Outline



Revision History

Major changes since the last revision

| Page or Reference | Description of change |
|-------------------|---------------------------------------------|
| | Additional information and typo corrections |
| 4 | Pin configuration |
| 15 | Package outline |
| | |

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