# ESD9R3.3ST5G

## **Transient Voltage Suppressors** ESD Protection Diodes with Ultra-Low

## Leakage

The ESD9R is designed to provide ESD protection for ASSPs and ASICs used in ultra low current applications such as human body sensors. These devices have been designed for leakage under 1 nA from 0°C to 50°C when turned off. During an ESD event, these devices turn on to clamp the ESD to a safe voltage level for the IC. These devices have the added benefits of low capacitance for high speed data lines and small package size for space constrained designs.

## **Specification Features:**

- Ultra-Low Leakage < 1 nA
- Ultra-Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 3.3 V
- Response Time < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- This is a Pb-Free and Halogen-Free Device

### **Mechanical Characteristics:**

CASE: Void-free, transfer-molded, thermosetting plastic Epoxy Meets UL 94 V-0 LEAD FINISH: 100% Matte Sn (Tin) MOUNTING POSITION: Any QUALIFIED MAX REFLOW TEMPERATURE: 260°C Device Meets MSL 1 Requirements

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000–4–2 (ESD) Contact		±10	kV
Air		±15	
НВМ		±16	
Total Power Dissipation on FR–5 Board (Note 1) @ T <sub>A</sub> = 25°C	P <sub>D</sub>	150	mW
Storage Temperature Range	T <sub>stg</sub>	–55 to +150	°C
Junction Temperature Range	ТJ	-55 to +125	°C
Lead Solder Temperature – Maximum (10 Second Duration)	ΤL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $FR-5 = 1.0 \times 0.75 \times 0.62$  in.

See Application Note AND8308/D for further description of survivability specs.



## **ON Semiconductor®**

http://onsemi.com





SOD-923 CASE 514AB

## MARKING DIAGRAM



= Specific Device Code

M = Date Code

J

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
ESD9R3.3ST5G	SOD-923	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

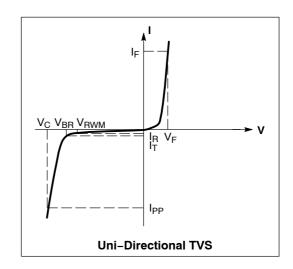
### **DEVICE MARKING INFORMATION**

See specific marking information in the device marking column of the Electrical Characteristics tables starting on page 2 of this data sheet.

## **ELECTRICAL CHARACTERISTICS**

 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$ 

Symbol	Parameter				
I <sub>PP</sub>	Maximum Reverse Peak Pulse Current				
V <sub>C</sub>	Clamping Voltage @ IPP				
V <sub>RWM</sub>	Working Peak Reverse Voltage				
I <sub>R</sub>	Maximum Reverse Leakage Current @ V <sub>RWM</sub>				
V <sub>BR</sub>	Breakdown Voltage @ I <sub>T</sub>				
Ι <sub>Τ</sub>	Test Current				
١ <sub>F</sub>	Forward Current				
V <sub>F</sub>	Forward Voltage @ I <sub>F</sub>				
P <sub>pk</sub>	Peak Power Dissipation				
С	Max. Capacitance @ $V_R = 0$ and f = 1.0 MHz				



\*See Application Note AND8308/D for detailed explanations of datasheet parameters.

ELECTRICAL CHARACTERISTICS	G (T <sub>A</sub> = 25°C unless otherwise noted, V <sub>F</sub> = 1.0 V Max. @ I <sub>F</sub> = 10 mA for all types)
----------------------------	--

		V <sub>RWM</sub> (V)	I <sub>R</sub> (nA) @ 1 V T <sub>A</sub> = 0°C to 50°C (Note 4)	V <sub>BR</sub> (V) @ I <sub>T</sub> (Note 2)	ե	С	(pF)	V <sub>C</sub> (V) @ I <sub>PP</sub> = 1 A (Note 5)	v <sub>c</sub>
Device	Device Marking	Max	Max	Min	mA	Тур	Max	Max	Per IEC61000-4-2 (Note 3)
ESD9R3.3ST5G	J*	3.3	1.0	4.8	1.0	0.5	0.9	7.8	Figures 1 and 2 See Below

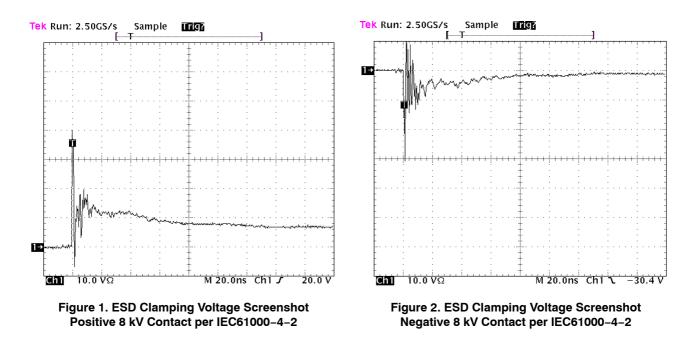
\*Rotated 270°.

2.  $V_{BR}$  is measured with a pulse test current I<sub>T</sub> at an ambient temperature of 25°C.

3. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

4. Limits over temperature are guaranteed by design, not production tested.

5.  $V_C$  measured using pulse waveform in Figure 5.



## ESD9R3.3ST5G

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)	
1	2	7.5	4	2	
2	4 15 8		8	4	
3	6	22.5	12	6	
4	8	30	16	8	

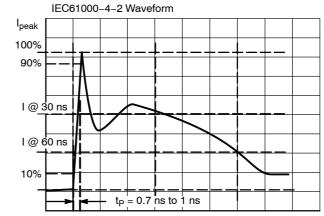


Figure 3. IEC61000-4-2 Spec

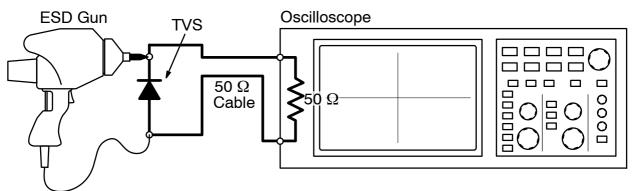


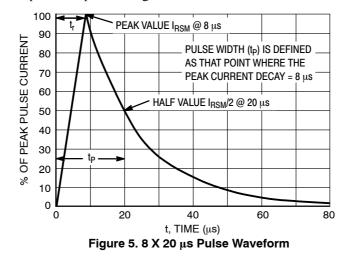
Figure 4. Diagram of ESD Test Setup

## The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

## **ESD Voltage Clamping**

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000–4–2 waveform. Since the IEC61000–4–2 was written as a pass/fail spec for larger

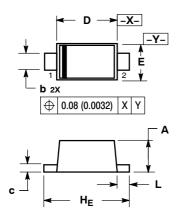
systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.



## ESD9R3.3ST5G

### PACKAGE DIMENSIONS

SOD-923 CASE 514AB-01 ISSUE B

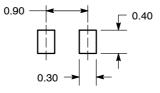


NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETERS.
  MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD
- FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.34	0.37	0.40	0.013	0.015	0.016	
b	0.15	0.20	0.25	0.006	0.008	0.010	
С	0.07	0.12	0.17	0.003	0.005	0.007	
D	0.75	0.80	0.85	0.030	0.031	0.033	
Е	0.55	0.60	0.65	0.022	0.024	0.026	
H <sub>E</sub>	0.95	1.00	1.05	0.037	0.039	0.041	
L	0.05	0.10	0.15	0.002	0.004	0.006	

#### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and use registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death agsociated with such unintended or unauthorized use patent solut. Cwas negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunit//Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5773-3850 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative